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Harnessing Energy from Electromagnetic Field: Practical Implementation Integrating Coil Antenna and IC Load

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ABSTRACT

An AC to DC voltage rectifier and its respective regulator were designed and integrated on a 0.25µm CMOS process. Its input impedance was measured along with the regulated DC output. Input impedance of a series of rectangular coil microstrip antenna on FR4 PCB with outer dimension of 78mm x 41mm was measured. The positive reactance of the antenna was matched at resonance with negative reactance of the integrated rectifier and regulator with addition of external capacitor. Relationship between incidental electromagnetic field in A/m at the coil microstrip antenna all the way to the rectified DC voltage at the output of the regulator is presented. In the context of wireless power transfer, this work focuses on the remote unit that absorbs electromagnetic field generated by another system and converts the energy into DC supply voltage for remote device

Keywords: Inductive coupling, wireless power, green energy, regenerative energy

INTRODUCTION

Wireless charging especially on mobile devices is a hot topic recently due to the convenience of replenishing battery power without lugging charger unit around. The wireless charging concept utilizing two coil antennas, one emanates electromagnetic field in area surrounding it while the other antenna absorbs the electromagnetic field and converts it into voltage.

This work focused on the second antenna, which will be called receiving antenna throughout this work, and necessary electronic components surrounding it to convert the electromagnetic field into alternating voltage. The antenna was designed in dimension that fits standard RFID tag for convenience of comparing the result with available standard. This work focuses on near field electromagnetic absorption; distance between electromagnetic field generator and the receiving antenna; open-source voltage

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generated at the receiving antenna at resonance and finally transforming the AC voltage at the receiving antenna into a DC voltage that can be used to power up electronic circuits. This work will only focus on 13.56MHz carrier frequency but the same concept can also work on other near field wavelength.

The electronic components required to convert the open-source voltage generated at the receiving antenna to DC voltage is voltage rectifier. The DC voltage resulted from the voltage rectifier can be used to power other electronic circuits. For this work, the type of voltage rectifier of interest is Dickson voltage doubler as it has been used in many other similar works as in Curty *et al.* (2005a, 2005b, 2005c) and Changming *et al*. (2006). To prevent the resulted DC voltage from growing indefinitely, a voltage regulator is necessary at the output of the rectifier.

For this work, the electronics circuits were designed and fabricated on a 0.25µm CMOS technology. The fabricated output is 1mm x 1mm integrated circuit (IC) loose die mounted on dedicated PCB. Input and output pads on the IC die is connected to input and output pads on the PCB using 1mil aluminum wire bond.

Simulation and measurement result on the receiving antenna coil for multiple of turns will be presented here. The most important measurement is the input impedances of the receiving antenna coil which will be presented here. This work will also present simulation and measurement result of the fabricated voltage rectifier and voltage regulator both on the functional operation of the electronics and its input impedance. Finally the voltage rectifier and voltage regulator will be combined and measured at resonance.

The voltage that appears at the input of the voltage rectifier is a divided voltage of open circuit voltage, V_{OC}, which resulted when an antenna coil is exposed to an electromagnetic field (Constantine, 1997). Additionally, effective distance of the receiving antenna to the electromagnetic generating antenna is also discussed.

CIRCUIT DESIGN

Voltage rectifier circuit used for this work is of type Dickson mainly due to many references to this architecture being used in CMOS process and near field electromagnetic field absorption such as in Curty *et al*. (2005a, 2005b, 2005c) and Changming *et al.* (2006). For this work, the voltage rectifier circuit which also widely referred to as voltage doubler is limited to two stages only.

It is given in Changming *et al.* (2006) that without voltage regulation, maximum output voltage from the voltage doubler is

$$V_{Out,\max} = 2N\left(V_{in,peak} - V_{th}\right) \quad [1]$$

where N is number of stages, V_{th} is threshold voltage across diodes D_1, D_2, D_3 or D_4 and $V_{in,peak}$ is the maximum amplitude of the divided V_{OC}. When a coil antenna enters an electromagnetic field, voltage appears across it. The voltage is called open-circuit voltage or V_{OC} in Constantine (1997). At the targeted cumulative load of I_{Load}, we want to have level of $V_{out,max}$ higher than the level of supply voltage we aim for. The excess electric charge is conditioned by voltage regulator to keep it at intended voltage level.

Schottky diode is preferred for diodes D_1, D_2, D_3 and D_4 as it has very low threshold voltage drop across it. For this work, the target foundry does not include Schottky diode in its list of supported device, thus diode-connected native NMOS is being utilized. Native NMOS device in this fabrication process has threshold voltage of only 0.1339v. Using equation 1 at input voltage of 650mv, $V_{out,max}$ of a two stages voltage doubler is 2.06v. This is more than enough as targeted output voltage for this work was at 1.1v.

The voltage doubler also has two DC block capacitors (C_{In1} and C_{In2}) of type Poly-insulator-Poly (PiP) at the input of the voltage doubler, one for each stage. The purpose is to block any unwanted DC voltages at the input as operation of the voltage doubler is very dependant to the alternating amplitude level of the input voltage.

Capacitor at the output of each stage, namely C_1 and C_2 were designed using low voltage NMOS. The motivation of using NMOS as capacitor at the output is due to higher capacitance per square area as low voltage NMOS has very thin oxide that separates Poly and Source/Drain/Substrate. Total capacitance per square micron is calculated at 5.835fF, using CGSO, CGDO and Cbulk value provided by foundry. In comparison, capacitor C_{In1} and C_{In2} which uses PIP capacitor only have 1fF per square micron. Additionally metal wires can be interlaced to add additional capacitance per square area.

For this work, value of capacitor C_1 and C_2 were selected at 267.76pF and 5251.52pF respectively for I_{Load} of between 25µA to 50µA. The values selected were the most optimum for the targeted I_{Load} level for final size of less than 1mm^2. Additionally voltage supply level does not drop by more than 10% during 100% ASK modulation. Having voltage supply level to drop too low will cause headroom issue in some internal circuits.

At the output of the rectifier, there are two diode-connected NMOS devices (D_{Reg1} and D_{Reg2}) in series acting as clamp-down circuit. This will limit output voltage of the rectifier to twice the threshold voltage of the diode connected NMOS device. Without the clamp-down voltage regulator, output voltage of the rectifier circuit can go up to $V_{out,max}$ level depending on load I_{Load}.

For this work, threshold voltage of the NMOS being used as diode in the clamp-down is around 550mv. Having two diode-connected NMOS acting as forward-biased diode towards common ground limits output of the voltage rectifier at around 1.1v.

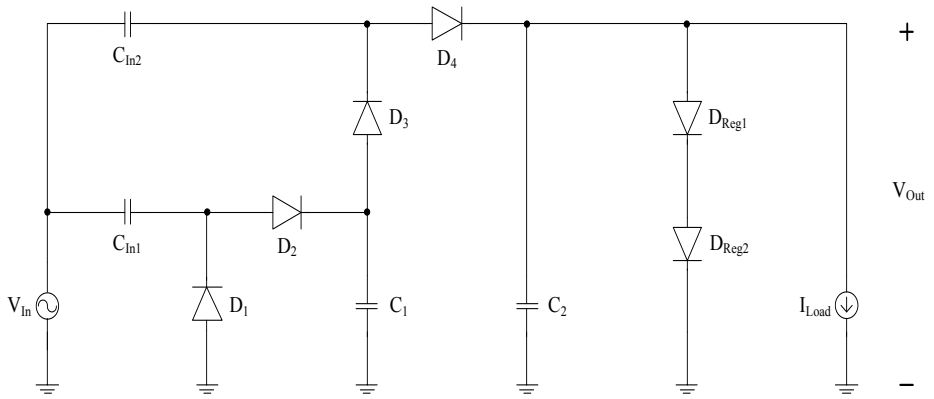

Fig.1: Rectifier and regulator circuit

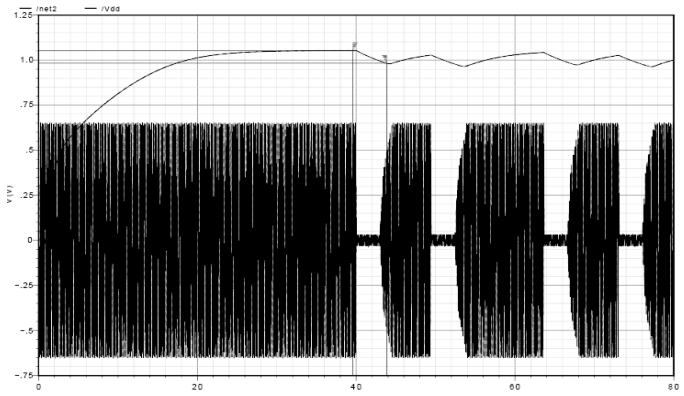

Fig.2: A 2-stage rectifier voltage doubler with C1=267.76pF and C2=5251.52pF regulated at 1.07v

MEASUREMENT RESULT

The die received from foundry was in a 5mm x 5mm form with 12 identical sub-dice. The main die was then sent for sub-dicing process.

Final results are loose IC die of interest with dimension of 1mm x 1mm. The dice was then mounted on a purposely built PCB with pads opening for wire bonding. The choice of bonding wire was a 1mil aluminum wire. On the PCB, input pads of the IC which is meant to be supplied with an AC voltage is connected to an SMA connector while output of the IC which is meant to be at DC level is connected to a PCB via for measurement. Fig.3 shows micrograph of the pre sub-diced IC dice received from the foundry.

Fig.4 shows an assembled module with one of the loose die mounted on the PCB, its input and output pads wire-bonded to the PCB with trace to elements for measurement such as SMA to supply input signal and output DC voltage measured on copper pad PCB via opening.

Characteristic of the IC is then measured in two ways. The first was to find relationship between voltage level at the input and its respective rectified and regulated output. For this work a sinusoidal signal generator was connected to the input of the IC through the SMA connector. The input signal was set at 13.56MHz frequency as it is a widely used frequency for Near-Field Electromagnetic transmission. Each signal level at the input is recorded as well as the respective DC output. Result is shown in Fig.5.

The first measurement was on the DC level of V_{Out} per $V_{In,peak}$. Rectification process did happened on silicon, but regulation did not. During design process, rectification was targeted at around 1.1v DC with the help of voltage regulator diodes but from the graph above it is shown that voltage regulation did not happen. Although rectification did happened, but input voltage required for the same 1v DC output is higher. In the simulation only about 650mv-peak input voltage required to get to the target DC voltage, but in silicon about 3v-peak input voltage needed.

One possible explanation for this issue is the diode connected native NMOS device for D_1, D_2, D_3 and D_4 in Figure 1 may have threshold voltage too low that it allows backflow of charges in the opposite direction, which is called reverse current. Reverse current negates

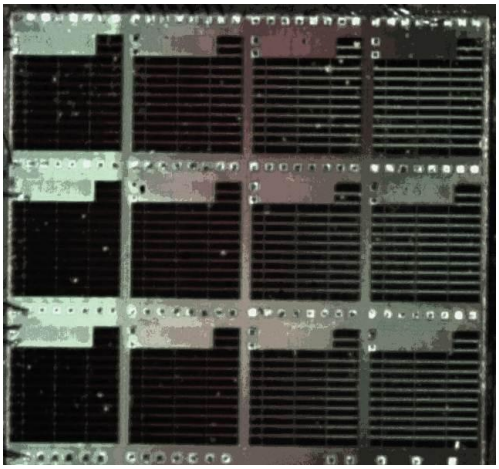

Fig.3: Fabricated Die

Fig.4: Subdiced IC mounted on PCB with SMA connector

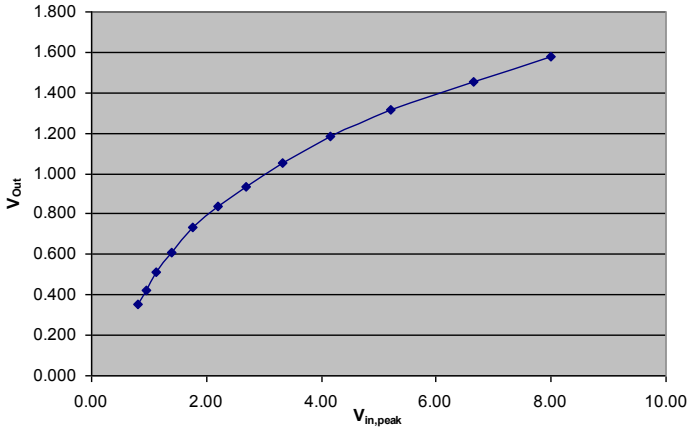

Fig.5: Plot of measured rectified and regulated voltage output as AC voltage at input is gradually increased

charge accumulation done in earlier part of the cycle. Only when the input level is way higher, the reverse current effect can be overcame by having much more forward current.

The voltage regulator circuit was designed to clamp output at about 1.1v for 650mv input signal level. If the reverse current is the cause of mismatch between simulation and physical, the voltage regulator now need to channel out to ground a much larger charge than it was designed for. It would be an uphill battle.

The diode connected native NMOS device was selected due to the low threshold voltage characteristic for optimum charge accumulation in the voltage doubler circuit especially at capacitor C2. Similarity between Schottky diode and diode connected native NMOS device end there though. Characteristic of a Schottky diode is it allows forward current to flow in exponential rate beyond its threshold voltage, while keeping reverse current low in reverse voltage. A diode connected native NMOS device also allows forward current to flow at exponential rate, but has much higher reverse current. Interestingly, this characteristic did not appear in simulation.

Another possible explanation for the big mismatch between simulation and silicon can be pointed out at an effort on layout to add more capacitance per square micron by interlaying metal layers. Since the metal interlaying was done at the layout stage without simulation model, there is no error-checking method available to trigger an alarm if shorts happened.

The metal interlaying was done as shown in Fig.7. Active and diffusion layer of NMOS which being used to create capacitors C1 and C2 in Figure 1 is connected to the Metal1 layer. The Metal1 layer is purposely laid right above poly layer of the NMOS to add more capacitance

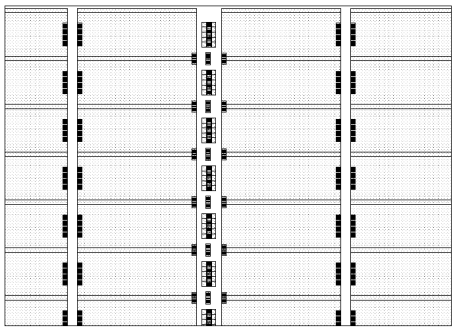

Fig.6: Metal1 and via1

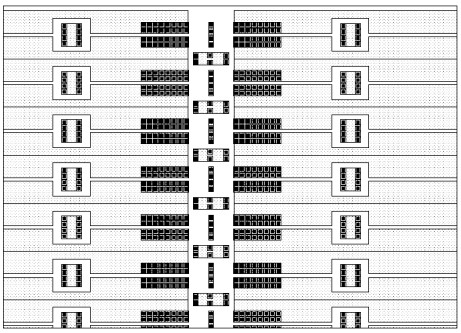

Fig.7: Metal2 and via2

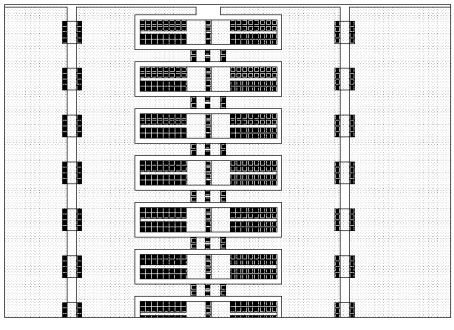

Fig.8: Metal3 and via3

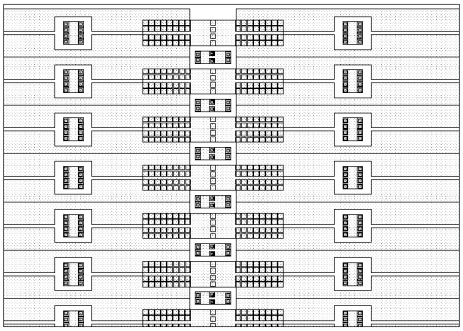

Fig.9: Metal 4 and via4

between Poly layer and active and diffusion layer. The Metal1 layer then allowed to tunnel through Metal2 to arrive at Metal3 layer at many points. Poly layer of the NMOS also tunnels through Metal1 to arrive at Metal2. Having Metal2 being laid everywhere there is Metal1, more capacitance is added to the C1 and C2 capacitor. The pattern continues till the top metal layer.

COIL ANTENNA DESIGN AND MEASUREMENT

A series of microstrip coil antenna were designed on single-layer FR4 type PCB. Dimension of its outermost turn is 78mm x 41mm with trace width kept at 0.5mm. The antennas were designed from one turn to 10 turns with pitch of 0.5mm and simulated using electromagnetic field simulator. Input impedance of the simulated result of each antenna was recorded and their equivalence inductance values at 13.56MHz frequency were recorded as well. The result is shown in Fig.10 indicated by diamond marker. Measured input impedance of the antenna coil is saved in soft copy in the form of Touchstone format with .s1p extension for further investigation.

To validate the result, three antennas with two, six and ten number of coils were fabricated and measured. Input impedance value of each fabricated coil was measured and recorded. The result is shown in Fig.10 indicated by triangle marker. It is confirmed that result of the actual antenna coil matches closely of simulation. Fig.11 shows measurement of six coil antenna on spectrum analyzer.

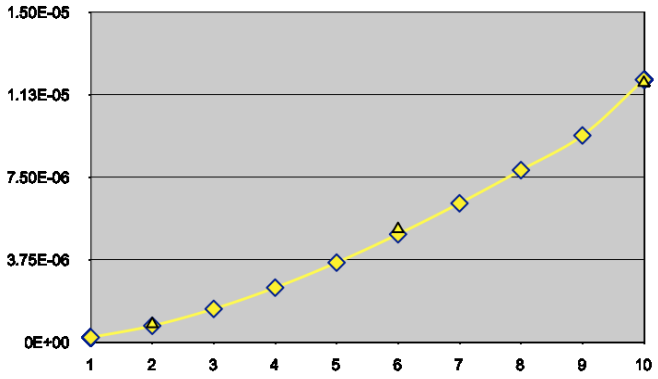

Fig.10: Inductance of simulated rectangular microstrip coil at various number of turns with measured results to validate

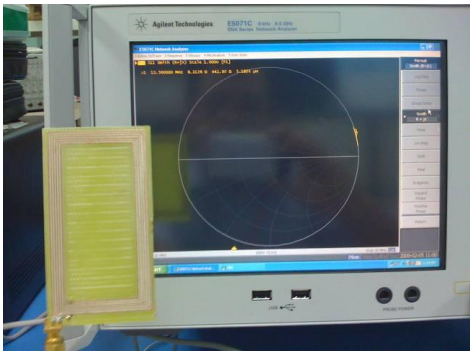

Fig.11: Measurement of fabricated antenna

THEORY

Equivalent circuit of the antenna coil and the fabricated IC is shown in Fig.12. The resistance R_L and capacitance C_L is the component of the integrated circuit input impedance while the capacitance C_{Coil}, R_{Coil} and L_{Coil} are components of the antenna coil.

The integrated rectifier and regulator circuit designed and fabricated as described in Figure 1 is modeled as R_L and C_L in Fig.12. From measurement, the value of R_L is known at 194.4Ω while value of C_L is known at 131pF at 13.56MHz frequency. In contrast, based on simulation data, value of R_L is at 348.07Ω while value of C_L is at 58.93pF at 13.56MHz frequency.

At resonance, all reactance of components C_L, C_{Coil} and externally connected C_{Ext} is a complex conjugate of reactance value of L_{Coil}. What's left are real impedance R_L and R_{Coil}. The final circuit at resonance is as in Fig.13. Finding V_L, input voltage to the integrated circuit is just a matter of voltage divider.

According to Constantine (1997), when an electromagnetic plane waves impinges upon a coil antenna, an open circuit voltage developed. The open circuit voltage is referred to as V_{OC} and shown in Fig.13. The supply voltage V_{OC} is defined in Constantine (1997) as

$$V_{OC} = j\omega V_{oc} = j\omega\ \pi a^2 B * N \qquad [2]$$

where πa^2 is the area inside the circular coil, N is number of turns in the coil and B is the incident magnetic flux density. Since for this case, rectangular coil antenna is used instead, some deliberate modification to the equation is needed. Also, most literature describes generated

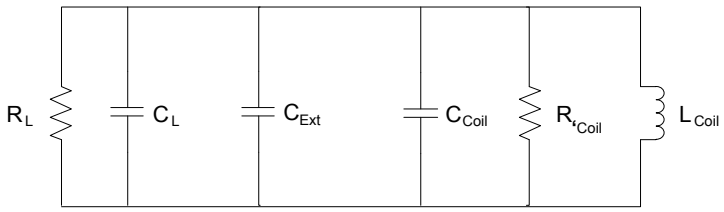

Fig.12: Equivalence circuit using Thevenin's

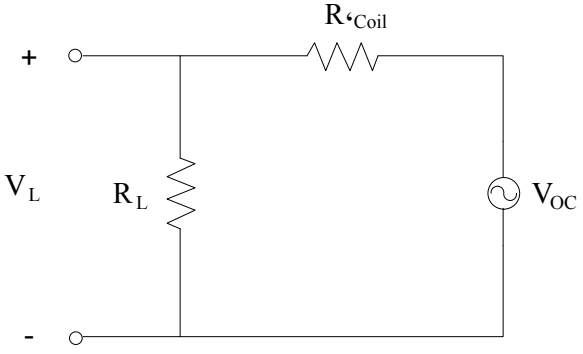

Fig.13: Equivalence circuit at resonance

field in electromagnetic field (H) term more than in magnetic field (B) term. Thus, the final V_{OC} equation that will be used here is

$$V_{OC} = j\omega\ \pi_0 H_{eff} * \Sigma A_n \quad [3]$$

where n is the number of turn, A_n is area of the rectangle of interest and μ_0 is vacuum permeability. At H_{eff} of 3A/m (rms), V_{OC} for each turn case is presented in Table 1.

TABLE 1
Area of antenna at each turns of coil and expected V_{OC}

N	A	V_{OC} (rms)	V_{OC} (p-p)
5	1.37×10^{-2}	4.41 v	6.24 v
4	1.14×10^{-2}	3.67 v	5.19 v
3	8.90×10^{-3}	2.86 v	4.04 v
2	6.16×10^{-3}	1.98 v	2.80 v
1	3.20×10^{-3}	1.03 v	1.45 v

For better understanding on distance between the field generating antenna and receiving antenna, ISO 10373-7 standard is used for some insight. In the standard, the field generating antenna for testing is defined as a circular coil with two turns and radius of 150mm. The standard also defined that typical operating distance as 37.5mm at H of 150mA/m rms. Using Biot-Savart equation as below

$$H = \frac{(I\,N\,R^2)}{2\sqrt{(R^2+z)^3}} \quad [3]$$

where R is the radius of the coil, N is number of turns and z is the distance from center of the coil perpendicular to the plane of the coil.

Rearranging the equation reveals that to get the electromagnetic field strength of 150mA/m as described in the standard require 0.55 Ampere of AC current injected into the coil. Rearranging the equation again, this time for distance z, we have a plot as in graph as in Fig.14.

IC AND ANTENNA INTEGRATION

As mentioned in the Theory section, V_L, the input voltage to the integrated circuit is a divided voltage of V_{OC}. For that reason this section is dedicated to establishing value of R_{Coil} at resonance. Since value of R_L is known from measurement, ratio of V_L to V_{OC} can be established easily.

In the spirit of saving time and cost, further measurements were done in system simulator. Touchstone file format of each component which was stored during measurement stage can be read by system simulator such as ADS. External capacitor, C_{Ext}, was added to the input port of the receiving antenna's Touchstone model in system simulator. The C_{Ext} is parallel to the

inductor L_{Coil} to add to the total complex conjugate that matches the inductance of the coil. Varying the external capacitor C_{Ext}, we will get pure real resistance (R_{Coil}) and zero reactance to the system.

Since real part of input impedance (RL) of the IC is known at 42kΩ, the divided voltage level VL can be estimated. Table 2 summarize it.

TABLE 2
Summary of V_L(p-p) at Varying Coil Inductor Turns

N	C_{Ext}	R_{Coil}	V_{OC}(p-p)	V_L(p-p)
5	36.55pF	9.15 x 10^4 Ohm	6.24 v	1.96 v
4	52.75pF	5.29 x 10^4 Ohm	5.19 v	2.30 v
3	86.20pF	2.60 x 10^4 Ohm	4.04 v	2.50 v
2	166.60pF	9.53 x 10^3 Ohm	2.80 v	2.28 v
1	512.32pF	1.74 x 10^3 Ohm	1.45 v	1.39 v

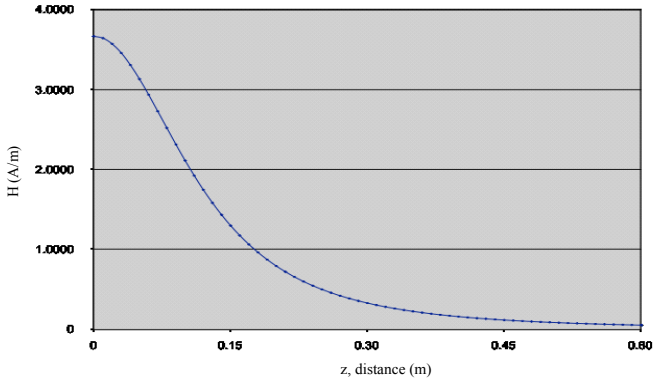

Fig.14: Distance from center of electromagnetic field generating antenna to specific distance (m) with respect to electromagnetic field (A/m)

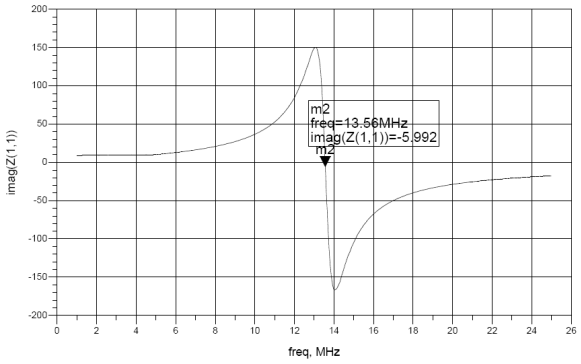

Fig.15: Total reactance

CONCLUSION

The main target of this work which to identify voltage at the input of rectifier at any given effective electromagnetic field has been achieved. Also, if the parameters as defined in equation [4] are known, distance between electromagnetic field generating coil antenna and the receiving antenna can be calculated.

Although there are mismatch between data from simulation and silicon, on the integration part the integrated circuit still usable in giving us some idea on improving the design further. Now it is known that V_L is a divided voltage of V_{OC}. Thus for future work, input resistance of the rectifier IC need to be made bigger for higher divided voltage in the integrated antenna-IC system.

In the target application for such a system, it is important to maximize V_L at any given V_{OC}. Also in the same time, for any given electromagnetic field level, we want to maximize V_{OC}. The relationship has been described between antenna coil area and V_{OC} in equation 3 for future improvement.

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